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09/620,474	07/20/2000	Makoto Fujiwara	43889-964	3082

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EXAMINER	
SHARON, AYAL I	

ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 06/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/620,474	FUJIWARA, MAKOTO	
	Examiner	Art Unit	
	Ayal I Sharon	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 March 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *7-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *7-13 and 17-27* is/are rejected.

7)☒ Claim(s) *14-16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 November 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Introduction

1. Claims 7-27 of U.S. Application 09/620,474 filed on 07/20/00 are presented for examination. The application has a foreign priority date of 07/30/1999. In Applicants' most recent request for reconsideration, filed 03/29/2003, no claims have been amended, no claims have been added, and no claims have been cancelled.
2. In Applicants' previous amendment, (paper #10, filed 10/17/2003), claims 7-19 were elected for examination by the Applicant in response to the restriction of paper #9. Non-elected claims 1-6 were cancelled. Claims 7,9,11,17,18,19 were amended. Claims 20-27 were added.
3. Examiner notes that none of the recommendations cited in the interview summary, dated 03/17/2004, were implemented.

Claim Objections

4. Claims 14-16 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. The prior art used for these rejections is as follows:

7. Mahmud, S.M. "Communication Performance in a Hierarchical Bus System". Int'l Symposium on Circuits and Systems, 1989. May 11, 1989. Vol.1, pp.122-125. (Henceforth referred to a "**Mahmud_1**").

8. Amadori, S. et al. "Design of Complex Systems with a VHDL Based Methodology". Proc. European Design Automation Conf. 1992. pp.658-663. (Henceforth referred to a "**Amadori**").

9. Hopper, A. et al. "Multiple vs. Wide Shared Bus Multiprocessors." Int'l Conf. on Computer Architecture, 1989. pp.300-306. (Henceforth referred to a "**Hopper**").

10. Mahmud, S.M. "Performance Analysis of Multilevel Bus Networks for Hierarchical Multiprocessors". IEEE Transactions on Computers. July 1994. Vol.43, Issue 7, pp.789-805. (Henceforth referred to a "**Mahmud_2**").

11. **Claims 7, 9, 12-13, 17, 19-21, and 23-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mahmud_1 in view of Amadori.**

12. In regards to Claim 7, Mahmud_1 teaches the following limitations:

> analyzing a number of collisions of bus transaction through operation simulation where said applications are operated by said control function part by successively using each of said plural libraries as the operation model of each of said plural applications.

(Mahmud_1, especially: Fig.6-8 and associated text; Tables 1 and 2. Examiner finds that a 11 conflicts" due to a "blocked" bus is equivalent to a "collision". Examiner finds that bandwidth is therefore a function of the number of collisions.)

However, Mahmud_1 does not expressly teach the use of using a database storing plural libraries corresponding to operation models of plural applications, from the preamble of the claim:

7. (Currently amended) A method of designing an interface for Connection between a control function part of a semiconductor integrated circuit and plural applications by using a database storing plural libraries corresponding to operation models of said plural applications, comprising a step of:

Amadori, on the other hand, teaches the uses of VHDL component models (See section 2, "Modeling of Standard Components"), and more specifically, that of Bus-functional models (Section 2.2) and the Buses as components (Section 2.4).

Amadori also expressly teaches that "... we forced all the designers to access a common, unique library in order to avoid dangerous duplication of equivalent models ..." This implies a database of operation models of different components / applications.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Mahmud_1 with those of Amadori, because "The design of complex systems requires a solid methodology in order to avoid dangerous anarchy during the design phase and to increase the overall quality of the final product." (See Amadori, Abstract).

13. In regards to Claim 9, Mahmud_1 teaches the following limitations:

analyzing a number of concurrent instruction processing through operation

simulation where said applications are operated by said control function part by successively using each of said plural libraries as the operation model of each of said plural applications. (Mahmud_1, especially: Fig.6-8, Tables 1 and 2 and associated text. Examiner finds "concurrent instruction processing" is inherent in a multi-processor, multi-memory system)

However, Mahmud_1 does not expressly teach the use of using a database storing plural libraries corresponding to operation models of plural applications, from the preamble of the claim:

9. (Currently amended) A method of designing an interface for connection between a control function part of a semiconductor integrated circuit and plural applications by using a database storing plural libraries corresponding to operation models of said plural applications, comprising a step of:

Amadori, on the other hand, teaches the uses of VHDL component models (See section 2, "Modeling of Standard Components"), and more specifically, that of Bus-functional models (Section 2.2) and the Buses as components (Section 2.4).

Amadori also expressly teaches that "... we forced all the designers to access a common, unique library in order to avoid dangerous duplication of equivalent models ..." This implies a database of operation models of different components / applications.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Mahmud_1 with those of Amadori, because "The design of complex systems requires a solid methodology in order to avoid dangerous anarchy during the design phase and to increase the overall quality of the final product." (See Amadori, Abstract).

14. In regards to Claim 12, Mahmud_1 teaches the following limitations:

(a) setting plural main parameters for ultimately evaluating said semiconductor integrated circuit and setting plural sub-parameters affecting each of said main parameters;
(Mahmud_1, especially: Fig.3, Fig.6-8, Tables 1 and 2, and associated text.)

(b) selecting library groups where said main parameters meet target values by evaluating each of said main parameters on the basis of said sub-parameters of each of said libraries; and
(Mahmud_1, especially: Fig.3, Fig.6-8, Tables 1 and 2, and associated text.)

(c) determining an interface by selecting an optimal library group by evaluating plural main parameters determined with respect to each of said selected library groups.
(Mahmud_1, especially: Fig.3, Fig.6-8, Tables 1 and 2, and associated text.)

However, Mahmud_1 does not expressly teach the use of using a database storing plural libraries corresponding to operation models of plural applications, from the preamble of the claim:

12. (Original) A method of designing an interface for connection between a control function part of a semiconductor integrated circuit and plural applications by using a database storing plural libraries corresponding to operation models of said plural applications and plural bus structures, comprising the steps of:

Amadori, on the other hand, teaches the uses of VHDL component models (See section 2, "Modeling of Standard Components"), and more specifically, that of Bus-functional models (Section 2.2) and the Buses as components (Section 2.4).

Amadori also expressly teaches that "... we forced all the designers to access a common, unique library in order to avoid dangerous duplication of equivalent models ..." This implies a database of operation models of different components / applications.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Mahmud_1 with those of Amadori, because "The design of complex systems requires a solid methodology in order

to avoid dangerous anarchy during the design phase and to increase the overall quality of the final product." (See Amadori, Abstract).

15. In regards to Claim 13, Mahmud_1 teaches the following limitations:

13. (Original) The method of designing an interface of Claim 12, further comprising, before the step (a), a step of analyzing said sub-parameters of each of said libraries through operation simulation conducted by successively using each of said plural libraries as an operation model of each of said plural applications.
(Mahmud_1, especially: Fig.3, Fig.6-8, Tables 1 and 2, and associated text.)

16. In regards to Claim 17, Mahmud_1 teaches the following limitations:

(a) successively selecting each of said plural libraries as the operation model of each of said plural applications;
(Mahmud_1, especially: Fig.3, Fig.6-8, Tables 1 and 2, and associated text.)

(b) operating said plural applications by said control function part, and analyzing performances of said control function part, an interface and said applications attained by using each of said libraries;
(Mahmud_1, especially: Fig.3, Fig.6-8, Tables 1 and 2, and associated text.)

(c) repeatedly conducting the steps (a) and (b), whereby determining an interface by selecting an optimal library group on the basis of results of the analysis; and
(Mahmud_1, especially: Fig.3, Fig.6-8, Tables 1 and 2, and associated text.)

(d) synthesizing an optimal interface on the basis of said determined parameters.
(Mahmud_1, especially: Fig.3, Fig.6-8, Tables 1 and 2, and associated text.)

However, Mahmud_1 does not expressly teach the use of using a database storing plural libraries corresponding to operation models of plural applications, from the preamble of the claim:

17. (Currently amended) A method of designing an interface for connection between a control function part of a semiconductor integrated circuit and plural applications by using a database storing plural libraries corresponding to operation models of said plural applications and plural bus structures, comprising the steps of:

Amadori, on the other hand, teaches the uses of VHDL component models (See section 2, "Modeling of Standard Components"), and more

specifically, that of Bus-functional models (Section 2.2) and the Buses as components (Section 2.4).

Amadori also expressly teaches that "... we forced all the designers to access a common, unique library in order to avoid dangerous duplication of equivalent models ..." This implies a database of operation models of different components / applications.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Mahmud_1 with those of Amadori, because "The design of complex systems requires a solid methodology in order to avoid dangerous anarchy during the design phase and to increase the overall quality of the final product." (See Amadori, Abstract).

17. In regards to Claim 19, Mahmud_1 teaches the following limitations:

19. (Currently amended) The method of designing an interface of Claim 17,

wherein in the step (b), a number of concurrent instruction processing occurring by operating said applications without any management by said control function part is analyzed with respect to each of said libraries, and a portion where the number of concurrent instruction processing is larger than a predetermined value is determined, and
(Mahmud_1, especially: Fig.3, Fig.6-8, Tables 1 and 2, and associated text.)

in the step (d), a cross bar bus is disposed in a bus where the number of concurrent instruction processing is larger than the predetermined value.
(Mahmud_1, especially: Figs.1-3, and p.122, col.1.)

18. In regards to Claim 20, Mahmud_1 teaches the following limitations:

20. (New) A method of designing an interface of an LSI including a bus structure, said LSI executes plural applications, the method comprising the steps of:

analyzing a performance of the bus structure through operation simulation for at least one of said plural libraries, where said specified application is operated for said specified bus structure; and
(Mahmud_1, especially: Fig.3, Fig.6-8, Tables 1 and 2, and associated text.)

determining a bus structure of said LSI in view of the result of said analyzing step.

(Mahmud_1, especially: Fig.3, Fig.6-8, Tables 1 and 2, and associated text.)

However, Mahmud_1 does not expressly teach the use of using a database storing plural libraries corresponding to operation models of plural applications, from the preamble of the claim:

> creating plural libraries, each library contains information of one specified application of the plural applications and one specified bus structure of said LSI;

Amadori, on the other hand, teaches the uses of VHDL component models (See section 2, "Modeling of Standard Components"), and more specifically, that of Bus-functional models (Section 2.2) and the Buses as components (Section 2.4).

Amadori also expressly teaches that "... we forced all the designers to access a common, unique library in order to avoid dangerous duplication of equivalent models ..." This implies a database of operation models of different components / applications.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Mahmud_1 with those of Amadori, because "The design of complex systems requires a solid methodology in order to avoid dangerous anarchy during the design phase and to increase the overall quality of the final product." (See Amadori, Abstract).

19. In regards to Claim 21, Mahmud_1 teaches the following limitations:

> 21. (New) The method of designing an interface of Claim 20,
> wherein said result of said analyzing step includes a number of collisions of bus transaction occurring.

(Mahmud_1, especially: Fig.6-8 and associated text; Tables 1 and 2. Examiner finds that a 11 conflicts" due to a "blocked" bus is equivalent to a "collision". Examiner finds that bandwidth is therefore a function of the number of collisions.)

20. In regards to Claim 23, Mahmud_1 does not teach the following limitations:

23. (New) The method of designing an interface of Claim 7, wherein the operation simulation is performed without any management.

Amadori, on the other hand, teaches that "... Although the model of the bus doesn't correspond to any physical device, its availability allows for testing the base cycles from the first phases of the design. The model is not only a debugging tool, but also allows one to try different architectural solutions." (See Amadori, p.661, left column).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Mahmud_1 with those of Amadori, because "This solution offers a smart alternative to the manual generation of stimulus patterns ..." (See Amadori, p.661, left column).

21. In regards to Claim 24, Mahmud_1 does not teach the following limitations:

24. (New) The method of designing an interface of Claim 9, wherein the operation simulation is performed without any management.

Amadori, on the other hand, teaches that "... Although the model of the bus doesn't correspond to any physical device, its availability allows for testing the base cycles from the first phases of the design. The model is not only a debugging tool, but also allows one to try different architectural solutions." (See Amadori, p.661, left column).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Mahmud_1 with those of Amadori,

because "This solution offers a smart alternative to the manual generation of stimulus patterns ..." (See Amadori, p.661, left column).

22. In regards to Claim 25, Mahmud_1 does not teach the following limitations:

25. (New) The method of designing an interface of Claim 13, wherein the operation simulation is performed without any management.

Amadori, on the other hand, teaches that "... Although the model of the bus doesn't correspond to any physical device, its availability allows for testing the base cycles from the first phases of the design. The model is not only a debugging tool, but also allows one to try different architectural solutions." (See Amadori, p.661, left column).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Mahmud_1 with those of Amadori, because "This solution offers a smart alternative to the manual generation of stimulus patterns ..." (See Amadori, p.661, left column).

23. In regards to Claim 26, Mahmud_1 does not teach the following limitations:

26. (New) The method of designing an interface of Claim 17, wherein the step (b) of operating said plural applications is performed without any management.

Amadori, on the other hand, teaches that "... Although the model of the bus doesn't correspond to any physical device, its availability allows for testing the base cycles from the first phases of the design. The model is not only a debugging tool, but also allows one to try different architectural solutions." (See Amadori, p.661, left column).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Mahmud_1 with those of Amadori,

because "This solution offers a smart alternative to the manual generation of stimulus patterns ..." (See Amadori, p.661, left column).

24. In regards to Claim 27, Mahmud_1 does not teach the following limitations:

27. (New) The method of designing an interface of Claim 21, wherein the operation simulation is performed without any management.

Amadori, on the other hand, teaches that "... Although the model of the bus doesn't correspond to any physical device, its availability allows for testing the base cycles from the first phases of the design. The model is not only a debugging tool, but also allows one to try different architectural solutions." (See Amadori, p.661, left column).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Mahmud_1 with those of Amadori, because "This solution offers a smart alternative to the manual generation of stimulus patterns ..." (See Amadori, p.661, left column).

25. Claims 8, 18, and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mahmud_1 in view of Amadori and further in view of Mahmud_2.

26. In regards to Claim 8, Mahmud_1 does not express the use of FIFOs as claimed in the following limitations:

8. (Original) The method of designing an interface of Claim 7, further comprising a step of generating FIFOs in a number of stages according to the number of collisions of bus transaction,
(Mahmud_2, especially: Fig.5, and associated text.)

wherein the number of collisions of bus transaction is analyzed with the FIFOs virtually inserted between said applications.
(Mahmud_2, especially: Fig.5, and associated text.)

Mahmud_2. on the other hand, does expressly teach the generation and analysis of buffers ("FIFOs"). (See especially: Fig.5, and associated text - Section IV.B. "Queuing Model of an Asynchronous MLB System").

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Mahmud_1, with those of Mahmud_2, because "if read and write references are treated equally ... the entire system behaves like a simple closed-queuing network. But if read and write references are treated differently, the queueing network model becomes a little bit complicated due to the presence of both open and closed class customers . ... It is obvious that more throughput can be obtained from the system if read and write references are treated differently than [if] they are treated equally." (Mahmud_2, p.796, col.1).

27. In regards to Claim 18, Mahmud_1 teaches the following limitations:

18. (Currently amended) The method of designing an interface of Claim 17,
wherein, in the step (b), a number of collisions of bus transaction occurring by operating said applications without any management by said control function part is analyzed with respect to each of said libraries, and
(Mahmud_1, especially: Fig.3, Fig.6-8, Tables 1 and 2, and associated text.)

However, Mahmud_1 does not express the use of FIFOs as claimed in the following limitation:

in the step (d), FIFOs in a number of stages according to the number of collisions of bus transaction are inserted between said applications.

Mahmud_2, on the other hand, does expressly teach the generation and analysis of buffers ("FIFOs"). (See especially: Fig.5, and associated text - Section IV.B. "Queuing Model of an Asynchronous MLB System").

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Mahmud_1, with those of Mahmud_2, because "if read and write references are treated equally ... the entire system behaves like a simple closed-queueing network. But if read and write references are treated differently, the queueing network model becomes a little bit complicated due to the presence of both open and closed class customers . ... It is obvious that more -throughput can be obtained from the system if read and write references are treated differently than [if] they are treated equally." (Mahmud_2, p.796, col.1).

28. In regards to Claim 22, Mahmud_1 does not express the use of FIFOs as claimed in the following limitation:

22. (New) The method of designing an interface of Claim 21, wherein said determining step includes inserting FIFOs in a number of stages according to the number of collisions of bus transaction.

Mahmud_2, on the other hand, does expressly teach the generation and analysis of buffers ("FIFOs"). (See especially: Fig.5, and associated text - Section IV.B. "Queuing Model of an Asynchronous MLB System").

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Mahmud_1, with those of Mahmud_2, because "if read and write references are treated equally ... the entire system behaves like a simple closed-queueing network. But if read and write references are treated differently, the queueing network model becomes a little bit complicated due to the presence of both open and closed class customers . ... It is obvious that more -throughput can be obtained from the

system if read and write references are treated differently than [if] they are treated equally." (Mahmud_2, p.796, col.1).

29. Claims 10-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mahmud_1 in view of Amadori and further in view of Hopper.

30. In regards to Claim 10, Mahmud_1 does not expressly teach the following limitations:

10. (Original) The method of designing an interface of Claim 9, wherein a structure of a cross bar bit is determined in accordance with the number of concurrent instruction processing.

Hopper teaches (See Abstract) that "The processors are connected to the memory through caches that snoop one or more shared buses in a crossbar arrangement".

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Mahmud_1 with those of Hopper, because Hopper has "... simulated a number of configurations in order to assess the relative performance of multiple versus wide bus machines, with various amounts of prefetch." (See Hopper, Abstract), while Mahmud_1 teaches that "... These results show show that a hierarchical bus structure would be a cost effective bus structure as compared to conventional multiple bus and peripheral bus structures." (See Mahmud_1, Abstract).

31. In regards to Claim 11, Mahmud_1 does not expressly teach the following limitations:

11. (Currently amended) The method of designing an interface of Claim 10, further comprising the steps of:

determining a portion where the number of concurrent instruction processing is larger than a predetermined value: and

generating a DMA and/or at least one cross bar bus to be disposed in a bus where the number of concurrent instruction processing is larger than the predetermined value, wherein the number of concurrent instruction processing is analyzed with the DMA and/or at least one cross bar bus disposed in the bus.

(Applicants define a "DMA" in the specification (p.24) as "The DMA (direct memory access) has a transfer function to allow direct data transfer between an input/output controller and a main storage not through the CPU.")

Hopper teaches (See Abstract) that "The processors are connected to the memory through caches that snoop one or more shared buses in a crossbar arrangement".

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Mahmud_1 with those of Hopper, because Hopper has "... simulated a number of configurations in order to assess the relative performance of multiple versus wide bus machines, with various amounts of prefetch." (See Hopper, Abstract), while Mahmud_1 teaches that "... These results show show that a hierarchical bus structure would be a cost effective bus structure as compared to conventional multiple bus and peripheral bus structures." (See Mahmud_1, Abstract).

Response to Arguments

Re: Priority

32. In regards to the priority date of the application, Examiner has found Applicant's comments filed 03/29/2004, and declaration filed xx/xx/xxxx regarding the priority to be persuasive. The priority date of the application is 07/30/1999. Examiner notes that the cited prior art in the current rejections predate the foreign priority date.

Re: Claim Rejections - 35 USC § 103

33. In regards to independent claims 7, 9, 12, 17, and 20, Applicants argue in p.2, para.4 of the amendment filed on 03/29/2004 that:

> ... in order to analyze an interface, the present invention can simulate ***actual*** operation of a semiconductor integrated circuit. In contrast, Mahmud 1 is a technical paper directed merely to ***theoretical*** simulation.

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., "actual" versus "theoretical" simulation) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

34. In regards to the independent claims, Applicants argue of the amendment filed on 03/29/2004 that:

> However, it is respectfully submitted that Amdori does not overcome the deficiencies of Mahmud 1. VHDL is merely a conventional modeling language used to design ***architecture*** rather than ***applications***. (p.3, para.2)
>
> Generally speaking, an "application" is a particular job which is executed by software, hardware, or a combination thereof. In this regard, an aspect of the present invention includes designing a kind of architecture of the processor ***according to an application(s)*** which is executed by the processor. (p.3, para. 4)
>
> In contrast, "architecture" is merely the structure of hardware. (p.4, para.1)

However, Applicants' arguments in the amendment appear to directly contradict the claim language. In claim 7, for example, the preamble reads as follows (emphasis added):

> A method of designing an ***interface*** for connection ***between a control function part of a semiconductor integrated circuit and plural applications*** by using a database storing plural libraries corresponding to operation models of said plural applications, ...

Given that the interface that is being designed is connected on one end to a control function part of a semiconductor integrated circuit (in other words – a hardware component), it follows to reason that the other end(s) of the interface will also be connected to hardware components. In other words, the claimed "applications" are hardware components, and not "hardware, software, or a combination thereof" as argued by the Applicants in the amendment.

Therefore, since libraries of code written in the VHDL language are commonly used to design / model / test designs of hardware components, the Amdori reference is relevant to the claimed invention. Moreover, even if not expressly taught in Amdori, it is inherent that a VHDL compilation software

package such as Synopsys can "simulate actual operation" of a VHDL design (see recent amendment, p.5, para.1).

35. In addition, based on the language in claim 7, which refers to modeling an interface that connects a control unit in an integrated circuit to 'applications', Examiner interpreted the method as being for designing a bus interface between a CPU and other hardware components. Support for this interpretation is found in Fig.9, which is described in the specification (p.11) as:

> Figure 9 is a diagram for showing part of a bus structure resulting from providing a cross bar bus in a portion where a large number of concurrent instructions occur in Embodiment.

Moreover, the Applicants provide additional support for this interpretation in the recent amendment (p.4, paragraph 2), with the statement that:

> As an intended use of the present invention, in a processor, for example, a bus connects plural components (where each component has a specific function) ...

36. The Applicants refer to Figures 6 and 7 in order to differentiate the claimed invention from the Amdori reference (see recent amendment, p.4, para.3), and more specifically, to differentiate "application" from "architecture".

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., "actual application" versus "operation model") are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

37. In regards to the Examiner raising the issue of "... possible relevance of prior art (as of yet un-cited) related to large scale network design to processor design" in the interview: Examiner notes that "processor design" is not a feature in independent claims 7, 9, 12, 17. The claimed invention refers to an "interface for connection between a control function part of a semiconductor integrated circuit and plural applications", and makes no reference to either processor or network design. There is no limitation restricting the "applications" to be on the same integrated circuit as the "control unit" and the "interface". Therefore, Examiner finds that prior art from the networking field could read upon the invention as presently claimed.

Examiner finds Applicants arguments to the contrary (recent amendment, p.4, para.2) to be unpersuasive. Applicants argue that a network connects "terminals" where each "terminal" does not have a specific function and is operationally independent of other terminals.

First of all, there is no limitation in the current claims restricting the "applications" to a "specific function" (which in and of itself is a vague definition).

Moreover, Applicants' argument is simply not correct. One example of a network that connect hardware components with "specific functions" is a control system network, where a CPU is connected to sensors or controllers.

38. In regards to the motivation to combine the the Mahmud 1 and Amadori references (see recent amendment, p.5, para.4), Applicants argue that the combination is improper because "... even assuming ***arguendo*** that Amadori

disclosed application-containing libraries, the cited prior art nonetheless would not suggest using such application libraries in actual operation simulations for interface design. Rather, at best, the cited prior art would still only suggest theoretical simulation of the applications."

Examiner respectfully disagrees. Examiner finds that libraries of VHDL models of circuit can be used in operation simulations. Examiner cites the following paragraph (Section 2.4 Buses, col.1, para.1) from the Amadori reference as support for this conclusion:

> During the project of a board based on a system bus (e.g. EISA, VME, ...) the possibility to simulate the bus itself and the patterns that pass along it can help the designer very much. Although the model of the bus doesn't correspond to any physical device, its availability allows for testing the base cycles from the first phases of the design. The model is not only a debugging tool, but also allows one to try different architectural solutions. The availability of this kind of model is mandatory when other parts of the system are under development, even the external partners. ... it's also possible to simulate interactions at the system level, even if the models of different system blocks are unavailable.

It is in light of the above cited teaching of Amadori that the Examiner respectfully disagrees with the Applicants' assertion that "the cited prior art nonetheless would not suggest using such application libraries in actual operation simulations for interface design."

Conclusion

39. Applicants are reminded of the comments in the interview summary. Examiner reiterates the comments in the interview summary that the teachings in Figures 6 and 7 represent subject matter not taught in the cited prior art and also not

claimed in the present claims. Moreover, Examiner reminds the Applicants that the scope of the current claims applies also to networks.

40. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Correspondence Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ayal I. Sharon whose telephone number is (703) 306-0297. The examiner can normally be reached on Monday through Thursday, and the first Friday of a biweek, 8:30 am – 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska can be reached on (703) 305-9704. Any response to this office action should be mailed to:

Director of Patents and Trademarks
Washington, DC 20231

Hand-delivered responses should be brought to the following office:

4th floor receptionist's office
Crystal Park 2
2121 Crystal Drive
Arlington, VA

The fax phone numbers for the organization where this application or proceeding is assigned are:

All communications: (703) 872-9306

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist, whose telephone number is: (703) 305-3900.

Ayal I. Sharon

Art Unit 2123

June 3, 2004

KEVIN J. TESKA
SUPERVISORY
PATENT EXAMINER